Cover Letter to Commissioner for Patents

Applicant's response to EPO action (related to European stage of this PCT application) has been worked out after US National Application with it's original Amendment Document were mailed to USPTO.
In order to reduce USPTO examination workload, the Applicant has incorporated his response to the EPO action in the Amendment Document provided herein.
Therefore the Preliminary Amendment Document presented herein shall totally replace the original Amendment Document mailed to USPTO on the 27/December/2004 (for the purpose of entry into the US national phase based on the PCT/CA2003/000909).

Such replacing Preliminary Amendment Document comprises:
Explanations & Marked-up Copies emailed in "amendm_docum_marked-07nov18.pdf";
Drawings Amendments in "DRW-annotat & replac-07nov18.pdf".
Clean Copies emailed in "amendm_docum_clean-07nov18.pdf",

Such file "amendm_docum_marked-07nov18.pdf"contains:
1. Cover Letter
2. Replay to International Search Report;
3. Amendments Explanation;
4. Marked up copy of Specification Amendments
5. Marked up copy of Claims Amendments showing references to antecedent specification paragraphs and original claims.

Such file "DRW-replacem & annotat-07nov18.pdf" contains Replacement and Annotated Sheets

Such file "amendm_docum_clean-07nov18.pdf" contains:
1. Clean copy of Specification Amendments and Abstract;
1. Clean copy of Claims Amendments.

1. Replay to International Search Report (mailed by EPO on 25/Nov/2003)

Generally speaking; an evaluation of application's multilevel innovations may require more time than that assigned for such PCT preliminary non-substantive examination. Consequently; DSP MSP fundamental differences and contributions over conventional solutions have not been recognized by such examination.
Such DSP MSP break-through contributions include; by several times better noise immunity enabling 2x longer communication links (see the sub-section 2.2 "Patentability Explanation" provided further below).
Nevertheless some of the patents shown in the relevant documents list turned out to be relevant enough to show that some of original claims were to broad and not specific enough. Such PCT examination contribution has been recognized and thoroughly addressed by replacing original claims with the new claims shown in the "Claims Amendments" attached herein.

While replay concerning sufficiently close conventional solutions has been given in the attached amended part "BACKGROUND OF THE INVENTION", the remaining references given in the report are addressed below as they are not close enough to be discussed in the patent document without downgrading its quality.

The D1 is addressed in the "BACKGROUND OF THE INVENTION".

The D2 addressed in the "BACKGROUND OF THE INVENTION" where it is renumbered to D3.

The D3 (US 4,977,582 invented by Zelle Bruce at al) is limited to using delay lines for adjusting phase delay of transmitted data bits. However, D3 circuits
do not have any of the fundamental features of the present invention such as; continuity of entire pulse over-sampling necessary for amplitude glitches elimination, or high processing throughput necessary for calculating and processing lengths of transmitted pulses, or wave-form screening and adaptive noise filtering.
Therefore D3 can not have any significant relevance to the present invention if new claims are taken into the consideration.

The D4 (US 5,467,464 invented by Oprescu Florin at al) is limited to using a captured delay line for a de-skewer design. D4 circuits do not have any of the major features of the present invention which are essential for any measurements and processing of transmitted pulses lengths and for any data recovery.
Therefore D4 can not have any significant relevance to the present invention if new claims are taken into the consideration.

The D5 is addressed in the "BACKGROUND OF THE INVENTION", were it is re-numbered to D2.

The D6 (US 5,872,791 Propp David at al) is totally unrelated to the original claims 34-38 which define arithmetic division algorithm having nothing in common with the D6 data coding or error correction algorithms.

The D7 (EP 0 292 208 American Telephone & Telegram) is totally unrelated to the original claims 34-38 which define arithmetic division algorithm having nothing in common with the D7 bits stuffing into a transmitted data frame for synchronization purposes.

2. Amendments Explanation

2.1 Amendments of "Background Art"

The last two paragraphs of the Background Art represent merely estimate performance advantages versus conventional solutions, which are fully supported by this invention features and structures defined in the original description, claims and drawings.

Such performance estimates were placed in the Background Art not destined for a patentable subject matter, in order to advance the process into reviewing major inventive differences existing beyond initially seen similarities (such as merely linguistic similarity of US 5,872,791 and EP 0,292,208 cited in ISR as Category Y document for actually unrelated claims 34-38).

The amended penultimate paragraph of Background Art is supported by; original claims (5, 29, 39, 49, 65, 66) and specification (last paragraph of p.1 and 2nd paragraph of p.2 and last 3 paragraphs of p.5 and 2nd paragraph of p.8).
The amended last paragraph of Background Art is supported by; original claims (61-64) and specification (&3 of p.2 and last & of p.7 continuing into &1 of p.8).
The statement "eliminate all the above deficiencies of conventional solutions and enable significantly longer transmission distances" represents positioning difference only, between this invention and conventional solutions, which is obvious for those skilled in the art.
Since such resolution of the Background Art section cannot be patented, it cannot contribute any new subject matter either.

In order to communicate this invention contributions over newly discovered conventional solutions presented in the Background Art without adding to much of a new text to the original specification, the section "Patentability Explanation" is provided below.

2.2 Patentability Explanation

Since every edge detection provides exact re-timing of the whole received signal, such pulse lengths processing obviously never needs any phase locking.
Furthermore without any phase locking, based on an inexpensive local clock having frequency accuracy +/-30ppm, this invention provides phase jitter tolerance improvements over conventional solutions which are listed below: over 6 times better tolerance in a lower 1/3 of received signal bandwidth, and over 2 times better tolerance in the remaining upper 2/3.
Furthermore; since entire received wave-form is uniformly densely sampled and continuously filtered and processed, short glitches caused by high frequency amplitude noise are identified and filtered out before any detection of a valid edge takes place.
Since said exact re-timing is provided by every edge detection, this invention solution locks instantly and never requires any acquisition time what makes it ideal for all the burst type communication links.
Still other major contributions over conventional solutions include means; for noise filtering based on advanced screening and analysis of captured over-sampled wave-forms, and for using noise filtering masks for adaptive noise filtering before any data error could occur.
The listed above and shown in the specification advantages shall be able to double transmission distance while reducing error rates at the same time.
The mentioned above improvements required multilevel contributing inventions such as; multiplying processing throughput with multistage sequential processing synchronized with high resolution high speed sampling circuits (SSP), multiplying speed and accuracy of arithmetic division needed to decode number of data entities in a received long pulse (FBS) etc.

Such SSP secures unique ability to perform continuous over-sampling and calculating pulses lengths, for high frequency waveforms reaching 1/2 of technology's maximum clock frequency.
Such over-sampling and processing of high frequency waveforms is covered by the new claim 72

which specifies in its characterizing part the ability to communicate between synchronous parallel pipelines.
Such inter-pipeline communication ability differentiates the SSP from D3 by enabling such continuous waveform oversampling and pulse lengths processing, while D3 and other conventional solutions are limited to processing "window" sized separate signal intervals and to bit by bit data recovery relying on sensitive to jiiter phase alignment with transmitters clock.

Such synchronous parallel pipelines of claim 73 process alternating waveform intervals, wherein such intervals are sampled with mutually overlapping sub-clocks spaced by gate delay only while such alternating intervals are fed into the pipelines with frequencies reaching ½ of maximum clock frequency.
Therefore said communication between parallel pipelines, destined for IC deep-submicron technologies having ~50% process delay variations, required invention of sub-clock selection system by one order more accurate than conventional solutions.
Such novel apparatus enabling selection of pre-ordered sub-clocks sequences is defined by the CSS claim 87.
Such CSS defines sequential clock generator providing selections of sequences of mutually overlapping sub-clocks produced by serially connected gates driven by a sampling clock.
Such selective sequencing of the very close overlapping sub-clocks is essential; for achieving by one order greater accuracy of parallel pipelines timing, and for multiplying speed of solutions covered by claim 68 and multiple other claims.

New SSP claim 73 secures 2 unique features essential for continuous processing of long high-frequency waveforms; wherein:
the first such feature specifies communication between sequential stages of a singular pipeline processing separate "window" sized sub-intervals;
and the second feature specifies communication between neighbor stages of parallel pipelines processing such separate "window" sized sub-intervals;
wherein such inter-stage or inter-pipeline communication is essential for continuous processing of entire pulses having variable lengths, instead of being limited to processing fixed "window" sized intervals and to the bit by bit data recovery with all the conventional solutions deficiencies explained above.
Consequently at least one of such features is necessary in order to measure entire pulse lengths and/or to filter-out noise from entire waveform including noise glitches between "windows".

The first feature is specified by the second statement in the claim body;
"or performing…, wherein a result of one such basic operation performed earlier is used for processing a result of another basic operation performed later".
Such first feature specifies said communication between such sequential stages of singular pipeline since such entire pipeline is named as sequential processing stages throughout all the specification and the claims.
Therefore the first feature has to relay on additional buffering of a processing result of an earlier "window" (produced by an earlier basic stage operation), until such earlier buffered result can be processed together with a processing result of a later "window" (produced by a later basic operation).
The first feature is supported by the antecedent texts indicated by references inserted in the text of claim 73 shown in the marked up copy of new claims.

The second feature specifies communication, between such consecutive parallel pipelines (named parallel processing phases) processing such consecutive waveform "windows". The second feature is well supported by the original claims 18 and 19, as it is indicated in the marked up copy of Claims Amendments.

Furthermore such second feature represents narrowing of the original SSP claim 11 in response to the D3 discovered by ISA. Since the 3rd staement of new claim 73 specifies the same configuration (of parallel phase shifted pipelines built with serially connected stages) as the original claim 11; the 4th statement (supported by claims 18-19) narrows the subject matter of original claim 11.
Since the 4th statement merely narrows the original claim 11 in response to the D3 discovery and covers only subject matter supported in the original specification and claims, such 4th statement shall be admissible in accordance with rules & practices concerning claim amendments.

Dependent claim 82 specifies use of estimates of periodical skew accumulation for correcting pulse lengths detected (spec. &4-8/p.17).
The 3rd characterizing statement of claim 82 is supported; by &5/p.6, and by &5/p.17 wherein the term "registered number of sampling clocks" is used as synonymous with the term "lengths of data string detected". Furthermore; the 3rd statement merely narrows both the 2nd statement of orig. cl.50 and the 2nd statement of orig. cl.52 to cases related to PSA embodiment in &5-8/p.17.
For such reasons the 3rd statement shall be admissible as well.

The FBS of claim 84 (having dependent claims 85 and 86) enables maintaining last bit accuracy for very long divisions of pulse lengths by symbol lengths while using only 1-2 bit long divider terms enabling much greater processing speed.

2.3 Amendments of "Purpose of the Invention"

The 1st paragraph of the sub-sec.1 "Purpose of the Invention" (see new page 1c) has been brought into more clear conformity with the &2/p.8 and original claim 65 by replacing the term "to provide" with the more definite term "comprising" used in said &2/p.8 and claim 65, as it is referenced in the amendments copy.
Furthermore entire such sub-section 1 has been brought into better conformity with the rest of the specification and made more clear by copying to it the narrowed part of &2/p.1only (i.e. without adding any new subject matter), as it is shown in the amended and clean copies.

2.4 Amendments of "Description of the Preferred Embodiment" and FIG.3A

The "Description of the Preferred Embodiment" (&1-2/p.11) and the FIG.3A (connections between registers 11DFR, 12DFR, 21DFR, 22DFR and their arithmometers 11DFA1,12DFA1,21DFA1,22DFA1) have been corrected in order to bring them into compliance with the original "Summary of the Invention" and with the original claims. Such corrections are shown on new page 11 and new FIG.3A shown in the Annotated Sheet and Replacement Sheet provided in the file "DRW-annotat & replac-07nov18.pdf".

The intent implemented by such corrections has been clearly documented in original spec. &4-5/p.4, &4/p.6 and in cl.18, cl.19, cl.47; where it is said unambiguously that:

> "In order to allow said boundary extension, carry over bit or bits of an output register of said first filter stage of one phase shall be clocked-in into an output register of the first filter stage of a next phase together with filtering results of the next phase. Consequently the second filter stage of the next phase shall use the output register of the first stage for filtering a wave-form interval which extends through both said phases."

This content of the &4/p.6 is repeated 3 times more in the original spec. & claims.
Since such corrections are made in the only way available to conform with the original well evidenced intent, they shall be admissible.

Reference in &1/p.16 to a non-existent sec. "Phase Skew Accumulation" has been corrected to the originally intended reference to the existing section 5. named as "Periodical Skew Accumulation", and similarly &2/p.16 reference to non-existent circuit & section "Phase Skew Accumulation" has been corrected to the originally intended reference to the existing circuit & section both named as Periodical Skew Accumulation in the titles of FIG.3B and said sec.5.
Resulting clean and amended copies of page 16 are attached herein.

2.5 Amendments of Abstract

Abstract has been corrected by including some application areas covered by &2/p.1 in the "Field of the Invention", as shown in the amended and clean copies of new Abstract attached herein.

2.6 Amendments of Claims

New claims 68-87 (replacing original claims 1-67) are attached in two copies; a clean copy and a marked-up copy, wherein such marked-up copy shows antecedents of terms used in the new claims with reference signs to original claim-number [cl.Nr] and/or original specification paragraph-number / page number [&Nr/page.Nr].

Conclusion

Based on the thorough response to ISA report and the above clarifications, it is thus respectfully submitted that the invention taught and defined herein by the claims embodies patentable subject matter.

The Examiner is earnestly solicited to give favorable consideration to this application and pass it to allowance.

Respectfully submitted,

By: John W. Bogdan

Specification Amendments

Please replace the corresponding original parts with the amended parts provided below.

BACKGROUND OF THE INVENTION

Field of the Invention

This invention is directed to an analysis of a waveform for a telecommunication system or for a measurement equipment, and more particularly to a Digital Signal Processing of Multi-Sampled Phase (DSP MSP).

The DSP MSP allows waveform analysis, noise filtering, and data recovery for wireless, optical , or wireline transmission systems and measurement systems and for a wide range of data rates and waveform timings.

The invention further includes Sequential Data Recovery from Multi Sampled Phase (SDR MSP), which is a version of the DSP MSP, which provides clock and data recovery for optical communications.

Background Art

~~Present waveform analyzers and serial data receivers use an analog front end for signal filtering, data recovery, and for a generation of data recovery sampling clock. Therefore more expensive bipolar or BICMOS technologies are needed to achieve sufficient performance, and said present designs have rather limited noise filtering capabilities and are able to cover only narrow application areas.~~

~~Analog design problems are further compounded by lower supply voltages which cause insufficient voltage head-room in deep sub-micron IC's which are becoming dominant in today's and future electronics.~~

~~There was a need for a waveform timing analyzer and a digital method of signal analysis which will reduce cost and complexity by replacing said analog or BICMOS technologies with less expensive CMOS technologies, and will improve noise filtering and increase programmability of data analysis algorithms and improve reliability of data recovery functions.~~

Background art for this invention is represented by the documents listed below:

D1 (US 5,668,830 by Georgiu Christos John ET AL)

D2 (PCT/CA01/00723 invented by Bogdan);

D3 (US 2002/0009171 invented by Ribo);

D4 (US 5,592,125 by Williams).

The D1 is limited to using delay lines and most basic digital filters for removing phase noise of waveform edges. D1 circuits enable merely edge phase aligning and data re-timing on a bit per bit basis for data serializing/de-serializing only.
Consequently, D1 circuits do not have any of the fundamental features of the present invention such as; over-sampling and noise filtering from entire pulse [spec.&2/p.8 wherein "multisampling of every individual bit" is synonymous to "over-sampling"] necessary for elimination of noise occurring inside data pulses, or cumulative processing operations [spec.&4/p.5] necessary for measuring and processing lengths of transmitted pulses [spec.&2/p. 8], or adaptive signal processing using wave-form screening [spec.&3/p.7-&1/p.8].

The D2 solution created variety of high resolution phase capturing techniques which are useful for measuring phase skews between low frequency frames in high quality synchronization circuits. However these D2 phase capturing techniques have never been targeting any processing throughput which could be even close to that needed for communication signal processing.
Therefore besides said high resolution phase capture, the D2 solution has fundamentally different principle of operation and produces entirely different results.
Consequently D2 can not contribute to any processing of much higher frequency signals commonly used in communication links.

The D3 solution represents latest generation of clock and data recovery (CDR) circuits which over-sample in expected transition region in order to achieve some fractional improvements of jitter tolerance.
The D3 captures windows consisting of samples covering entire data bit interval.
Every such window covers single bit interval only and it is captured and processed separately from other windows on a bit interval by bit interval basis without any correlation between data captured in

consecutive windows. Such lack of correlation amounts to inability to filter out narrow glitches occurring between windows.

Therefore the D3 windows need to be centered around expected edges of received data bits in order to enable said bit by bit processing without data recovery errors.

Obviously such window centering can only be achieved by phase locking to the received signal.

Other over-sampling solution is the CDR with bang-bang phase detector (CDR with BBPD) represented by D4.

While taking more samples provides D3 with better base for jitter filtering than that of such CDR with BBPD, dynamics of D3 phase locking has to accommodate additional interference caused by said jiter filtering and by further processing of output data providing return reference for the D3 phase locked loop.

Similarly as the D3 and the CDR with BBPD, all other conventional solutions analyzers and receivers of serial data have the same common feature limiting severely their performances; they require phase locking to received signal in order to recover data based on sampling localized in a credible region of the received wave-form.

The phase locking requirement is not only difficult to achieve but furthermore it imposes significant limitations on receiver performances such as those listed below:

- Jitter tolerance is very low outside the bandwidth of receivers PLL while such PLLs bandwidth is usually below 1/10 of the bandwidth of transmitted signals which are the major sources of phase jitter and amplitude noise.
- Such receivers are defenseless against high frequency noise occurring in wave-form regions which can not be filtered out using said localized sampling.
- Such PLL based receivers require significant lock acquisition times before newly established data link becomes operational what is an impediment for all burst types of data links.

This invention is based on fundamentally different principle of operation relying on; measurements of pulse lengths [spec.&2/p.8, cl.66] of incoming wave-form [spec. &7-8/p.5, &5/p.6]] with accuracy matching single gate delays [spec. &4/p.2, &1/p.3], and on digital processing of such accurate pulse lengths [spec. &1-5/p.6] in order to recover data transmitted by the wave-form or to analyze the waveform [spec. &3,&8,&9/p.1, &2/p.8].

Such superior principle of operation combined with adaptive signal processing algorithms utilizing verification of received waveforms [spec. &2-3/p.2, &4/p.7-&1/p.8], eliminate all the above deficiencies of the conventional solutions and enable significantly longer transmission distances.

SUMMARY OF THE INVENTION

1. Purpose of the invention

It is an object of present invention to create a circuit for Digital Signal Processing of Multi-Sampled Phase (DSP MSP) ~~of a wave-form, and more particularly to provide~~ comprising [&2/p.8, cl.65] ~~a~~ circuits for Sequential Data Recovery from Multi Sampled Phase (SDR MSP)~~,~~ of an optically received wave-form.

The DSP MSP shall allow programmable comprehensive noise filtering and wave-form timing analysis for wave-forms ranging from lowest to highest frequencies.

The DSP MSP allows waveform analysis, noise filtering, and data recovery for wireless, optical , or wireline transmission systems and measurement systems ~~and for a wide range of data rates and waveform timings~~ [&2/p.1].

Specification Pages Amendments

Please replace the original page 11 of the Specification with the amended page 11 provided below:

In addition to the outputs of the digital filter arithmometers 11DFA1/12DFA1 of the phases 11/12: several carry over bits ~~(22DFA1(Cov)/21DFA1(Cov))~~ (22DFR(Cov)/21DFR(Cov)) from the ~~arithmometers~~ registers of the previous parallel phases 22/21, are re-timed into the digital filter registers 11DFR/12DFR by the clocks 11Clk1/12Clk1.
Similarly carry over bits ~~(11DFA1(Cov)/12DFA1(Cov))~~ (11DFR(Cov)/12DFR(Cov)) from the ~~arithmometers~~ registers of the phases 11/12, are re-timed into the digital filter registers 21DFR/22DFR.
Said carry over bits from the previous parallel phases allow the next third stage of the ~~DNF~~ SDR MSP to filter incoming wave-form pulses which extend beyond a boundary of a single capture register.

The 11DFR/12DFR are connected to the digital filter arithmometers 11DFA2/12DFA2 (see FIG. 3A), which are both fed to the digital filter register (1DFR) through the 2:1 selector (2:1SEL).
Similarly as for said second stage:
The programmable control unit (PCU) determines logical and/or arithmetical processing which the 11DFA2/12DFA2 shall perform, by pre-loading the filter control register (FCR2) with a control code which is applied to the 11DFA2/12DFA2.
Additionally the PCU determines the mask FMR2(R:0) which the pre-filtered data 11DFR/12DFR shall be processed against, by pre-loading the filter mask register (FMR2).

The 11SEL signal equal to 1/0 selects the 11DFA2(R:0)/12DFA2(R:0), to be downloaded to the phase one digital filter register (1DFR) by the clock 1Clk2 (see FIG.3A and ~~FIG.5A~~ FIG.2A).

4. Sequential Phase Control and Phase Processing Stages
The Sequential Phase Control is shown in the FIG.2B and the Phase1 Processing Stages 2 to 8 (1PPS) are shown in the FIG.3A.

The binary edge encoders (BEE) are implemented by the third stage of the SDR MSP, in order to convert filtered sampling data into binary encoded transition time of the filtered MW signal.

The phase1 front edge encoder (1FEE) detects a last transition of the MW during the sampling period, and produces a binary number of sampling clocks which occurred between the beginning of the sampling period and the last transition.

The phase1 end edge encoder (1EEE) detects a first transition of the MW during the sampling period, and produces a binary number of sampling clocks between the beginning of the sampling period and the first transition.

Whenever only one transition of the MW occurs during a sampling period (Ps), a difference of the 1FEE minus the 1EEE shall amount to 0.

If two transitions of the MW occur, the difference of the 1FEE minus the 1EEE shall amount to a positive nonzero number of sampling clocks which occurred between the transitions.

Please replace the original page 16 of the Specification with the amended page 16 provided below:

- a data bit is added to a data string which corresponds to the MW inter-transition interval (see Sec. "Received Data Collection");
- a phase skew, which is expected between a sampling clock period and a period of a received data bit, is added to the phase1 skew accumulator1 (1PSA1) as it is further explained in the Sec. "~~Phase~~ Periodical Skew Accumulation".

While the above mentioned functions are being performed by the Received Data Collection and by the ~~Phase~~ Periodical Skew Accumulation, outputs of the Phase Processing Stages (see FIG.3A) are ignored until the end of the string.

In order to explain operations of the Phase Processing Stages at the end of a data string, listed below estimates shall be made:

- the content of the above mentioned 1ESR2 never exceeds +/- Ps (where Ps is a sampling clock period), because the 1FER and 1EER can never exceed 1Ps value and the 1ESR2 is loaded with their subtraction result;
- the content of the 1PSA1 never exceeds +/- 1.2Ps, because eventual positive/negative 1PSA1 overflows are corrected by subtracting/adding an expected data bit period and increasing/decreasing number of data bits which are being collected.

When the end of the string is reached, the Phase Processing Stages perform functions which are explained below.

The 1FER is subtracted form the 1EER and the resulting phase skew between the front and end edges is transferred into the phase1 edge skew register2 (1ESR2).

The 1PSA1 and the 1ESR2 are added and the result, which is not greater than 2.2Ps, is loaded into the phase1 final skew register (1FSR).

The 1FSR content is evaluated for how many received data bits it corresponds to and used to modify lengths of the data string, as it is further explained below.

If 1FSR(P) = 1 indicates positive 1FSR content: 1FSR - 1.5Pe is loaded into the phase1 double length register (1DLR), and 1FSR - 0.5Pe is loaded into the phase1 single length register (1SLR)

(where the Pe is an averaged expected data bit period which is calculated and provided by the PCU).

A positive 1DLR content indicated by the 1DLR(P) = 1, shows that the 1FSR content shall be approximated to +2 data bits which need to be added to the data string by the Data Collection circuits.

A negative 1DLR content indicated by the 1DLR(P) = 0 and a positive 1SLR content indicated by the 1SLR(P) = 1, show that the 1FSR content shall be approximated to +1 data bits which need to be added to the data string by the Data Collection circuits.

When the 1SLR is negative, the 1SLR(P) = 0 indicates that the 1FSR content shall be approximated to 0 data bits and nothing is added to the data string by the Data Collection circuits.

If 1FSR(P) = 0 indicates negative 1FSR content: 1FSR + 1.5Pe is loaded into the phase1 double length register (1DLR), and 1FSR + 0.5Pe is loaded into the phase1 single length register (1SLR).

A negative 1DLR content indicated by the 1DLR(P) = 0, shows that the 1FSR content shall be approximated to -2 data bits and 2bits need to be subtracted from

Please replace the original page 29 of the Specification with the amended page 29 provided below:

At the beginning of the next time frame, which has 128 phase1 cycles, the last captured 1DDB content is further downloaded to the phase1 data register (1DDR) by the clock signal 1Clk3/128. Number of said mask detections is counted in the mask counter buffer (1MCB), as it is explained below:

- at the beginning of every time frame which has 128 phase1 cycles, the 1MCB is reset/preset to 0/1 if there isn't/is a mask detection for the first cycle of the frame which is signaled by the 1PHA/128ena = 1;
- the 1MCB is increased by 1 / kept the same, if there is / isn't any mask detection during a particular phase1 cycle;
- at the beginning of the next time frame, the 1MCB is downloaded to the phase1 mask counter register (1MCR) and the output of the 1MCB>0 decoder (MCB>0 DEC) is downloaded to the 1MCR(P) bit, by the 1Clk3/128.

Said 1DDR and 1MCR are read by the PCU, when the beginning of the next frame is communicated to the PCU by the phase1 128^{th} clock enable signal (1PHA/128ena) and the above mentioned 1MCR(P) = 1 indicates that at least 1 detection of a pre-selected mask occurred during the previous frame.

Said PCU controlled capturing of a wave buffer content is implemented, as it is explained further below.

The sample number register (SNR) is loaded by the PCU: with a phase number defined as phase1/phase2 if the SNR(0) is set 0/1, and with a particular phase cycle number in a time frame defined by SNR(7:1) bits.

Since there are 2 phases with 128 cycles per time frame, SNR(7:0) bits define 1 of 256 sampling cycles for having its wave buffer captured and made available for a further analysis by the PCU.

Said SNR is downloaded into the phase1 sample number buffer (1SNB) at the beginning of a time frame by the first phase1 clock of the frame 1Clk2/128.

At the beginning of a time frame: the phase1 sample number counter (1SNC) is set to 0, since the 1PHA/128ena selects 0 to be loaded into the 1SNC by 1Clk2.

During every other cycle of the time frame: 1 is added to the SNC content, since the 1PHA/128ena

is inactive during all the next cycles of the frame.

The 1SNC(7:1) and the 1SNB(7:1) are being compared by the logical comparator (Log.Comp.), which produces the Eq = 1 signal when their identity is detected.

Said Eq = 1 enables the 1SNB(1) = 0/1 to select the 11WB(R:0)/12WB(R:0) in the 3:1 selector (3:1 SEL), for capturing in the phase1 sampled data buffer (1SDB).

At the beginning of the next time frame, the output of the 3:1 SEL is additionally captured in the phase1 sampled data register (1SDR) by the signal 1Clk3/128.

Said 1SDR is read by the PCU, which is notified about availability of the requested sample by the signal 1PHA/128ena.

CONCLUSION

In view of the above description of the invention and associated drawings, other modifications and variations will now become apparent to those skilled in the art based on the teachings contained herein. Such other modifications and variations fall within the scope and spirit of the present invention.

Please replace the previous Abstract with the Abstract provided below.

Abstract

The DSP MSP invention provides an implementation of programmable algorithms for analyzing a very wide range of low and high frequency wave-forms.
The DSP MSP comprises a synchronous sequential processor (SSP) for real time capturing and processing of in-coming wave-form ~~and~~ including a programmable computing unit (PCU) for controlling SSP operations and supporting adaptive signal analysis algorithms. The DSP MSP further comprises a ~~circuit for~~ Sequential Data Recovery from Multi Sampled Phase (SDR MSP), for a receiver of an optical wave-form.

Claim Amendments

Please replace the previous claims with the claims listed below.

Claims 1-67 (canceled)

68. (new) A method of digital signal processing of multi-sampled phase (DSP MSP), recovering data from a received signal [cl.65], which comprises capturing multiple samples of the signal per a symbol time [cl.29] with a sampling clock or its sub-clocks defining known phase displacements versus the sampling clock [cl.29]; the DSP MSP method [&2/p.8] comprising the steps of:

detection of phases of rising and falling edges of the signal [cl.66] by using said signal samples captured at said known phase displacements [cl.29];

evaluation of a length of a pulse of the signal by using said phases of signal edges [cl.66];

calculation of a number of data bits received in the pulse by using said evaluation of the pulse length [cl.66].

69. (new) A method as claimed in claim 68 further comprising a processing of said captured signal, wherein said captured signal processing comprises:

utilizing multiple sequential processing stages, driven by the sampling clock or clocks synchronous to the sampling clock [&3/p.2, cl.1, cl.2];

utilizing multiple parallel processing phases, wherein consecutive parallel phases are driven by clocks which are shifted in time by one or more periods of said sampling clock [&3/p.2, cl.11];

passing outputs of a one parallel processing phase to a next parallel phase [&3/p.2, cl.18], wherein output register bits of the original parallel phase are re-timed by clocking them into an output register of the next parallel phase simultaneously with processing results of the next parallel phase [&3/p.2, cl.19];

using said passed outputs for processing conducted by a following sequential processing stage which belongs to the next parallel processing phase [&3/p.2, cl.18].

70. (new) A method of digital signal processing of multi-sampled phase (DSP MSP), recovering data from a received signal [cl.65], which comprises capturing multiple samples of the signal per a

symbol time [cl.29] with a sampling clock or its sub-clocks defining known phase displacements versus the sampling clock [cl.29]; the DSP MSP method [&2/p.8] comprising the steps of:

filtering out noise from said captured signal with digital filters [cl.67, &1-4/p.6];

detecting phases of rising and falling edges of the resulting filtered signal [cl.66] derived from said signal samples captured at said known phase displacements [cl.29];

evaluation of a length of a pulse of the filtered signal by using said phases of filtered signal edges [cl. 66];

calculation of a number of data bits received in the pulse by using said evaluation of the pulse length [cl.66].

71. (new) A method as claimed in claim 70, wherein said evaluation of pulse length comprises the steps of:

defining an edge skew, between an edge of the sampling clock and the signal edge, with the time displacement of sub-clock which captures a change in a signal level [cl.49];

measuring said pulse length as being composed of such edge skew of a front edge of the incoming waveform, an integer number of sampling clock periods between the front edge and an end edge, and such edge skew of the end edge of the waveform [cl.49].

72. (new) A method of digital signal processing of multi-sampled phase (DSP MSP) for recovering data from a received signal waveform, captured with a sampling clock or its sub-clocks [&2/p.8], by processing length of inter-transition intervals of the captured waveform [&7-9/p.11, &6-8/p.12]; the DSP MSP method comprising the steps of:

capturing multiple received signal levels during every symbol time by the sampling clock or its sub-clocks [&3/p.2, &2/p8, cl.29];

converting such captured data into transition times of the received signal waveform [&7-9/p.11];

measuring said length of inter-transition interval occurring between said transition times [&6-8/p.12, cl.66];

calculating a number of data bits received during the inter-transition interval by evaluating said lengths of inter-transition interval [&2/p.8, &6-8/p.12, cl.66].

73. (new) A method of synchronous sequential processing (SSP) for sampling and capturing and

processing of a waveform [cl.1, cl.4, cl.5], wherein said waveform sampling and capturing use a sampling clock or outputs of a sampling clock delay line [cl.4, cl.5] and said waveform processing uses multiple sequential processing stages [cl.1] or multiple parallel processing phases [cl.11]; wherein the SSP method comprises the steps of:

driving said sequential processing stages with clocks synchronous to said sampling clock,

and performing a cumulative processing operation split into a series of consecutive basic operations implementing addition or subtraction or comparison [spec.&4/p.5 and spec.&10/p.13 - &2/p.14 and FIG.3A] wherein a result of one basic operation performed earlier [such earlier operation result representing a front edge skew is preserved in 1FER until an end edge is detected after all the basic operations occurring in between, as shown in spec.&10/p.13 - &2/p.14 and FIG.3A] is used for processing [such processing shown in &1-2/p.14 and FIG.3A, calculates the phase skew between the front edge of the data string and the end edge] a result of another basic operation performed later [such later result representing an end edge skew is provided by 1EER when an end edge is detected after all the basic operations occurring in between, as shown in spec.&10/p.13 - &2/p.14 and FIG.3A];

or driving said parallel phases with clocks synchronous to said sampling clock wherein consecutive parallel phases are driven by clocks shifted in time by one or more periods of the sampling clock [cl.11],

and passing outputs of a one parallel phase to a next parallel phase in order to use said passed outputs for processing conducted by a following stage of the next parallel phase [spec. &4/p4, cl.18] wherein said outputs passing is performed by re-timing output register bits of the one phase by clocking them into an output register of the next parallel phase simultaneously with processing results of the next parallel phase [spec. &5/p4, cl.19];

wherein said use of earlier sequential operation result for processing later sequential operation result or said passing of outputs of one parallel phase to next parallel phase, enables continuous processing of indefinite waveform interval carrying high frequency pulses.

74. (new) An SSP method as claimed in claim 73 comprising merging of said parallel processing phases [cl.14], the SSP method comprising the step of:

merging said multiple parallel processing phases into a smaller number of parallel phases or into a single processing phase, when passing from a one sequential processing stage to a next sequential

stage[cl.14];

wherein clocking frequency of such merged phase equals to a sum of clocking frequencies of said parallel phases which are clocked into the merged phase [see &7/p.11 and FIG.3A showing merging of phase 11DFR clocked by 11Clk1 with phase 12DFR clocked by 12Clk1 into phase 1DFR clocked by 1Clk2, wherein 1Clk2_frequency =11Clk1_frequency +12Clk1_frequency].

75. (new) An SSP method as claimed in claim 73 further comprising synchronous sequential stages or parallel processing phases for noise filtering, the SSP method comprising the steps of:

clocking-in carry over bit or bits of an output register of a first filter stage of said one parallel phase into an output register of the first filter stage of the next phase together with filtering results of the next phase [spec.&4/p.6, cl.47];

using the output register of the first filter stage of one phase by a second filter stage of next phase for filtering a wave-form interval which extends through both said parallel phases [spec.&4/p.6, cl. 47].

76. (new) An SSP method as claimed in claim 73, wherein:

said sequential processing stages use selectors or arithmometers or output registers [cl.23].

77. (new) An SSP method as claimed in claim 76 wherein said waveform processing further comprises use of multiple parallel processing stages; wherein;

said multiple parallel processing stages, performing different logical or arithmetical operations, are driven by the same clock which is applied simultaneously to all the parallel stages [cl.20].

78. (new) An SSP method as claimed in claim 73 further comprising use of a programmable control unit (PCU)) for implementing programmable or adaptive signal processing algorithms [&2-3/p.2]; the SSP method comprising the steps of:

using said waveform processing, utilizing sequential processing stages or parallel processing phases, for real time capturing and processing of an in-coming waveform [spec.&2-3/p.2, cl.1];

using said PCU for reading results of the waveform processing from said synchronous sequential stages or parallel processing stages and for controlling operations of the waveform processing [&2-3/p.2, &1-2/p.6, &3-4/p.7, &1-4/p.28, cl.61-64].

79. (new) An SSP method as claimed in claim 78, the SSP method further comprising:
screening and capturing of the incoming signal with a wave-form screening and capturing circuits (WFSC) controlled by the PCU [spec.&1-4/p.28].

80. (new) An SSP method as claimed in claim 79, wherein the SSP method further comprises:
using said WFSC for verification of said captured waveforms for compliance or non-compliance with programmable patterns [cl.57] and for buffering captured waveform for which the preprogrammed compliance or said non-compliance has been detected [cl.59];
wherein said programmable patterns are provided by the PCU and such buffered waveform is read by the PCU [spec.&2-4/p.28]

81. (new) An SSP method as claimed in claim 79, wherein operations of said WFSC further comprise:
selecting a time interval for which incoming wave-form captures shall be buffered and communicated to the PCU, by programming a time slot selection circuit [cl.60, spec.&2-4/p.28];
wherein such slot selection is programmed by the PCU and such pre-selected buffered waveform is read by the PCU [spec.&2-4/p.28].

82. (new) An SSP method as claimed in claim 73 comprising use of a periodical skew accumulation (PSA) circuit [cl.51] for correcting cumulative error caused by periodical phase skews [&5-8/p.17]; the SSP method comprising the steps of:
using a periodical skew as an estimate of a phase skew between the sampling clock period versus an expected period of a clock which drives the incoming signal [cl.51];
using the PSA for calculating an accumulation of said periodical skews for a single pulse or for a combinations of pulses of the incoming signal [cl.51];
using such periodical skew accumulation to correct a length of a single data string or multiple data strings detected [this statement is supported by the &5/p.6, and by &5-8/p.17 wherein the term "registered number of sampling clocks" is synonymous with the term "lengths of data string detected". Furthermore this statement narrows 2nd statements in both cl.50 and cl.52 to cases related to PSA embodiment shown in spec.&4-7/p.16].

83. (new) An SSP method as claimed in claim 82; wherein operations of said PSA comprise the steps of:

reading a next set of said periodical skews from the PCU or other circuits [spec.&4/p.18] and attaching them to a present set of the periodical phase skews [cl.52];

synchronous communication of said accumulations of the pulse skews to phase processing stages [spec.&5-6/p.6] which use such accumulations to modify a lengths of said single data string or multiple data strings detected [spec.&4-7/p.16 and &5/p.17].

84. (new) A method of fractional bit staffing (FBS) for improving accuracy of fixed point arithmetic over that of conventional solutions [spec.&2/p.5] for a long cumulative processing operation split into a series of basic addition or subtraction or comparison operations [spec.&2-5/p.5, &5-8/p.17] between components of a processed argument [such as symbol time periods of said inter-transition interval of the received signal, named as Pe in &5-8/p.17] and terms of a processing argument [such as sampling clock periods of the inter-transition interval, named as Ps in &5-8/p.17]; the FBS method comprising the steps of:

expressing said processing argument as a series of terms, wherein each term may have a differently staffed last bit or several last bits expressing a fractional value of the term [&3-4/p.5 and &5-8/p.17 wherein differently staffed bits are included in the periodical phase skew (Ps-Pe)];

combining said staffed last bits with previous bits expressing more significant constant part of the term in order to provide said term [spec.&3-4/p.5];

a series of such terms is provided for a repeatedly performed arithmetic operation [&3-4/p.5, &5-8/p. 17, cl.34);

using every consecutive term, of a processing argument of said cumulative operation, for processing performed during a corresponding consecutive basic operation [spec.&3-4/p.5];

wherein the FBS enables reduction of a total error of such long cumulative operation to a single last bit resolution [spec.&4-5/p.5, &5-8/p.17];

85. (new) An FBS method as claimed in claim 84, wherein:

said series of multiple binary terms is downloaded to a register [cl.35];

a circuit which performs said arithmetic operations uses said terms

by shifting the register during any operation and accessing the same portion of the register [cl.35]

or by utilizing a selector circuit which selects a consecutive portion of the register which contains the corresponding term [cl.36].

86. (new) An FBS method as claimed in claim 84, comprising correction of cumulative errors in measuring lengths of incoming signal inter-transition interval with local sampling clock having periodical phase skews versus symbol periods expected in the incoming signal [&5-8/p.17]; wherein:

a series of said periodical phase skews is derived as estimates of a phase skew between a sampling clock period versus the expected symbol period anticipated for consecutive symbol periods sampled during the inter-transition interval, wherein such phase skew estimates may differ for said consecutive symbol periods [&5-8/p.17, cl.51];

the series of periodical phase skews, used as said differently staffed last bits expressing said fractional values, are combined with a sampling clock period, used as the more significant constant part of the terms, in order to produce said terms [&5-8/p.17, cl.51].

87. (new) A clock selection system (CSS) for enabling sub-clocks, generated by the outputs of serially connected gates which a sampling clock is propagated through, during particular phases [cl.9] corresponding to cycles of the sampling clock [cl.7]; wherein:

clock selectors connected serially are used for enabling said sub-clocks [cl.9, cl.13];

falling edges of said sub-clocks are used for driving said clock selectors selecting parallel processing phases during which positive sub-clocks are enabled [cl.9, cl.13];

or rising edges of said sub-clocks are used for driving said clock selectors selecting parallel processing phases during which negative sub-clocks are enabled [cl.9, cl.13].